

REMARKS

Claims 1-21 were pending in this application.

Claims 1-21 have been rejected.

No claims have been amended.

Claims 1-21 remain pending in this case.

Reconsideration and full allowance of Claims 1-21 are respectfully requested.

I. REJECTION UNDER 35 U.S.C. § 103

The Office Action rejects Claims 1-7 and 15-21 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,396,888 to Notani et al. ("*Notani*"). The Office Action rejects Claims 8-14 under 35 U.S.C. § 103(a) as being unpatentable over *Notani* in view of U.S. Patent No. 5,319,679 to Bagby ("*Bagby*"). These rejections are respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed.

Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142.

Notani recites a clock recovery circuit for use in a transmission system. (*Col. 18, Lines 25-26; Abstract*). In *Notani*, multiple "variable delay lines" (elements 71 through 7N) process clock signals and generate delayed clock signals. (*Col. 18, Lines 38-41*). The delayed clock signals are then fed through OR gates. (*Col. 18, Lines 41-44*).

First, Claims 1, 8, and 15 recite a "first current controlled delay line" and a "second current controlled delay line." While *Notani* recites the use of "variable delay lines," the variable delay lines are controlled based on a "control voltage" supplied by a loop filter. (*Col.*

18, Lines 34-41). *Notani* lacks any mention that the variable delay lines are controlled based on a current supplied by the loop filter. As a result, *Notani* fails to disclose, teach, or suggest multiple “current controlled delay lines” as recited in Claims 1, 8, and 15.

Second, Claims 1, 8, and 15 recite a “multiplier” for “multiplying” two signals to “thereby produce an output product signal proportional to a phase shift” between the signals. The Office Action asserts that the OR gate (element OGN) of *Notani* anticipates the “multiplier” recited in Claims 1, 8, and 15. (*Office Action, Page 2, Last paragraph*).

The OR gate of *Notani* does not produce an output signal that is “proportional to a phase shift” between two signals. Instead, the OR gate of *Notani* performs a logical OR operation involving a multiple clock signal (CKFPi) and a delayed multiple clock signal (DCKFPi) to produce a recovered clock signal (RCKi). (*Col. 18, Lines 40-44*). *Notani* contains no recitation that the recovered clock signal is “proportional to a phase shift” between two signals as recited in Claims 1, 8, and 15. As a result, *Notani* fails to disclose, teach, or suggest a “multiplier” for “multiplying” two signals to “thereby produce an output product signal proportional to a phase shift” as recited in Claims 1, 8, and 15.

Bagby is cited by the Office Action as allegedly disclosing demodulation circuitry. *Bagby* is not relied upon as disclosing, teaching, or suggesting any other elements of Claims 1, 8, and 15.

For these reasons, the Office Action has not established a *prima facie* case of obviousness against Claims 1, 8, and 15 (and their dependent claims). Accordingly, the Applicants respectfully request withdrawal of the § 103 rejection and full allowance of Claims 1-21.

II. CONCLUSION

For the reasons given above, the Applicants respectfully request reconsideration and full allowance of all pending claims and that this application be passed to issue.

SUMMARY

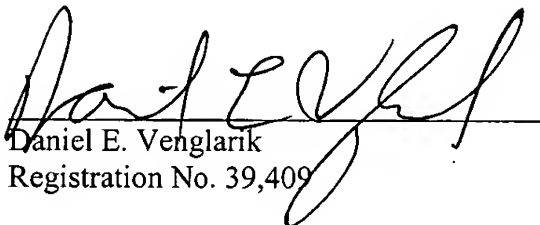
If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *dvenglarik@davismunck.com*.

The Commissioner is hereby authorized to charge any fees connected with this communication (including any extension of time fees) or credit any overpayment to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

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